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METHOD FOR FORMING INTERLAYER INSULATING FILM IN A SEMICONDUCTOR MANUFACTURING METHOD

[Bandochei jaezobangbeobui chunggan jeolyeonmak hyeongsong bangbeob]

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Brief description of the figures

Figure 1 is a schematic cross section showing the product obtained by the method for forming an interlayer insulating film as an application example of the present invention.

Figure 2 is a graph showing a stabilization process of source gases that are used in the interlayer insulating film formation of the present invention.

Figure 3 is a schematic cross section showing the product obtained by a conventional method for forming an interlayer insulating film.

Figure 4 is a graph showing a stabilization process of source gases that are used in the conventional interlayer insulating film formation.

Explanation of symbols

100	Substrate
200	Pattern
300	Silicon nitride film
400	BPSG layer
500	BSG layer

Detailed explanation of the invention

Purpose of the invention

Technical field of the invention and prior art

The present invention pertains to a method for manufacturing a semiconductor. In particular, the present invention pertains to a method for forming an interlayer insulating film in a semiconductor manufacturing method that first forms a BSG layer on a lower film utilizing the difference in the time in

which source gases of boron and phosphorus are stabilized and flow at the initial stage of an interlayer insulating film and can prevent the formation of voids and etching of the lower film by completing the interlayer insulating film.

When an inlayer insulating film (interlayer dielectric) is vapor-deposited, the film is initially vapor-deposited in a state in which boron (B) and phosphorus (P) are only flowing minimally, and during interlayer insulating film flow as a subsequent process, voids are generated by the difference in the flow velocity from the BPSG.

As a method to solve this problem, a method that flows and stabilizes triethyl borate (TEB) and triethyl phosphate (TEPO) as sources of boron and phosphorus has been introduced. However, in this case, a silicon nitride film as a lower film is also etched, so that the silicon substrate in an active region is oxidized.

The reason for this is that phosphorus and boron exist at the interface with a silicon nitride film through TEPO and TEB flowing at the initial stage of the vapor deposition of an interlayer insulating film, and phosphoric acid (H_3PO_4) is formed by H_2 and O_2 gases that are injected during the subsequent wet flow. The above-mentioned phosphoric acid is an etching substance of the silicon nitride film, and the phosphoric acid at the interface eventually etches the silicon nitride film, and if the etching is completed, the silicon substrate is oxidized by the O_2 gas. This phenomenon is illustrated in Figures 3 and 4.

Figure 3 is a schematic cross section showing the product obtained by a conventional method for forming an interlayer insulating film, and Figure 4 is a graph showing a stabilization process of source gases that are used in conventional interlayer insulating film formation.

In Figure 3, a silicon nitride film (30) is formed on a pattern (20) as the product obtained by a prescribed process on a substrate (10), and a BPSG layer (40) as an interlayer insulating film is formed on the above-mentioned silicon nitride film (30).

At that time, it can be understood that when the above-mentioned interlayer insulating film is formed, as shown in Figure 4, the film is initially vapor-deposited in a state in which boron and phosphorus flow minimally and during interlayer insulating film flow as a subsequent process, voids can be generated by the difference in the flow velocity from the BPSG.

Also, phosphorus exists between the BPSG as a vapor-deposited interlayer insulating film and the silicon nitride film as an etching stopper, and phosphoric acid is generated during the subsequent wet flow. It can be understood that the above-mentioned phosphoric acid has a structure that can etch the silicon nitride film.

Thus, when the interlayer insulating film is formed, voids are formed, and the oxidation of the silicon substrate is advanced by etching of the silicon nitride film with phosphoric acid, so that the characteristics of the semiconductor device is degraded.

Technical problems to be solved by the invention

Therefore, the purpose of the present invention is to provide a method for forming an interlayer insulating film in a semiconductor manufacturing method that first forms a BSG layer on a lower film utilizing the difference in the time in which source gases of boron and phosphorus are stabilized and flow at the initial stage of an interlayer insulating film and can prevent the formation of voids and etching of the lower film by completing the interlayer insulating film.

Constitution and function of the invention

In order to achieve the above-mentioned purpose, the method for forming an interlayer insulating film in a semiconductor manufacturing method of the present invention is characterized by the fact that it consists of a step that forms an etching stopper on a wafer to which a prescribed process has been applied; a step that flows at least two or more different source gases on the above-mentioned etching stopper and first forms a first insulating film with a prescribed thickness utilizing the difference in the time in which the above-mentioned source gases are stabilized; a step that forms a second insulating film on the above-mentioned first insulating film using the above-mentioned source gases; and a step that flows O_2 and H_2 under the conditions of a process temperature of 800-900°C and a process time of 10-60 sec on the above-mentioned final product.

At that time, the above-mentioned first insulating film is preferably a BSG layer vapor-deposited in a range of 10-150 Å, and the above-mentioned second insulating film is preferably a BPSG layer.

Next, a preferred application example of the present invention will be explained in detail referring to the attached figures.

Figure 1 is a schematic cross section showing a product obtained by the method for forming an interlayer insulating film as an application example of the present invention, and Figure 2 is a graph showing a stabilization process of source gases that are used in the interlayer insulating film formation of the present invention.

In Figure 1, a silicon nitride film (300) is formed on a pattern (200) as a resultant product to which a prescribed process has been applied on a substrate (100), and a BPSG layer (400) as an interlayer insulating film is formed on the above-mentioned silicon nitride film (300). At that time, the silicon nitride film (300) is vapor-deposited at about 100 Å, and the above-mentioned interlayer insulating film

is vapor-deposited at about 9.5 kÅ. Here, the above-mentioned silicon nitride film will act as an etching stopper later. It can be understood that the above-mentioned structure is the same as that of the prior art.

In the above-mentioned structure, since the silicon nitride film (300) is etched with phosphoric acid, as a characteristic of the present invention, a BSG layer (500) is further formed between the above-mentioned silicon nitride film (300) and the BPSG layer (400) as an interlayer insulating film.

In order to form the above-mentioned BSG layer (500), TEB as a source gas of boron is flowed in a stabilized state at the initial stage of the vapor deposition of the above-mentioned interlayer insulating film. This process is well shown in Figure 2.

As shown in Figure 2, it can be understood that the TEB has already been stabilized and flowed at about 200 sccm and TEPO is stabilized after about 9 sec and flowed at about 40 sccm. Here, TEOS is stabilized from the initial stage and flowed at about 600 sccm.

Under the above-mentioned conditions, it can be understood that the BSG layer is formed first on the silicon nitride film. The above-mentioned BSG layer is vapor-deposited at about 100 Å. Then, the BPSG layer is formed by the above-mentioned TEOS, TEB, and TEPO.

On the other hand, the above-mentioned resultant product is wet-flowed, and the above-mentioned wet flow is advanced at a process temperature of 830°C for a process time of 30 sec by flowing O_2 and H_2. At that time, in the prior art, phosphoric acid was formed by P found at the interface of the silicon nitride film and the BPSG layer, and the above-mentioned silicon nitride film was etched. However, in the present invention, the BSG layer is formed on the above-mentioned silicon nitride film by the above-mentioned process, and even if P exists at the interface of the above-mentioned BSG layer and BPSG layer, since phosphoric acid cannot etch the above-mentioned BSG layer, the silicon nitride film as the lower film is protected.

Also, it can be understood that void formation can be suppressed by flowing TEB as a source gas of boron in a stabilized state at the initial stage of the vapor deposition of the above-mentioned interlayer insulating film and stabilizing and flowing TEPO.

Thus, it can be understood that the void formation and the etching of the etching stopper can be prevented by setting the difference in the stabilization time of the source gases for forming the interlayer insulating film.

Effect of the invention

As mentioned above in detail, according to the method for forming an interlayer insulating film in the semiconductor manufacturing method of the present invention, with the formation of a BSG layer between an etching stopper and a BPSG layer as an interlayer insulating film, the etching stopper can be prevented from being etched with phosphoric acid generated during the wet flow.

Also, the formation of voids can be prevented by stabilizing and supplying the source gases of boron and phosphorus at a time difference. As a result, the yield can be improved by improving the characteristics of the semiconductor device.

It is evident that the present invention is not limited to the above-mentioned application example but can be variously modified by a person with ordinary knowledge in the corresponding field within the technical concept of the present invention.

Claims

1. A method for forming an interlayer insulating film in a semiconductor manufacturing method, characterized by the fact that it consists of a step that forms an etching stopper on a wafer to which a prescribed process has been applied; a step that flows at least two or more different source gases on the

above-mentioned etching stopper and first forms a first insulating film with a prescribed thickness utilizing the difference in the time in which the above-mentioned source gases are stabilized; a step that forms a second insulating film on the above-mentioned first insulating film by the above-mentioned source gases; and a step that flows O_2 and H_2 under the conditions of a process temperature of 800-900°C and a process time of 10-60 sec on the above-mentioned product.

2. The method for forming an interlayer insulating film in the semiconductor manufacturing method of Claim 1, characterized by the fact that the above-mentioned first insulating film is a BSG layer vapor-deposited in a range of 10-150 Å.

3. The method for forming an interlayer insulating film in the semiconductor manufacturing method of Claim 1, characterized by the fact that the above-mentioned second insulating film is preferably a BPSG layer.

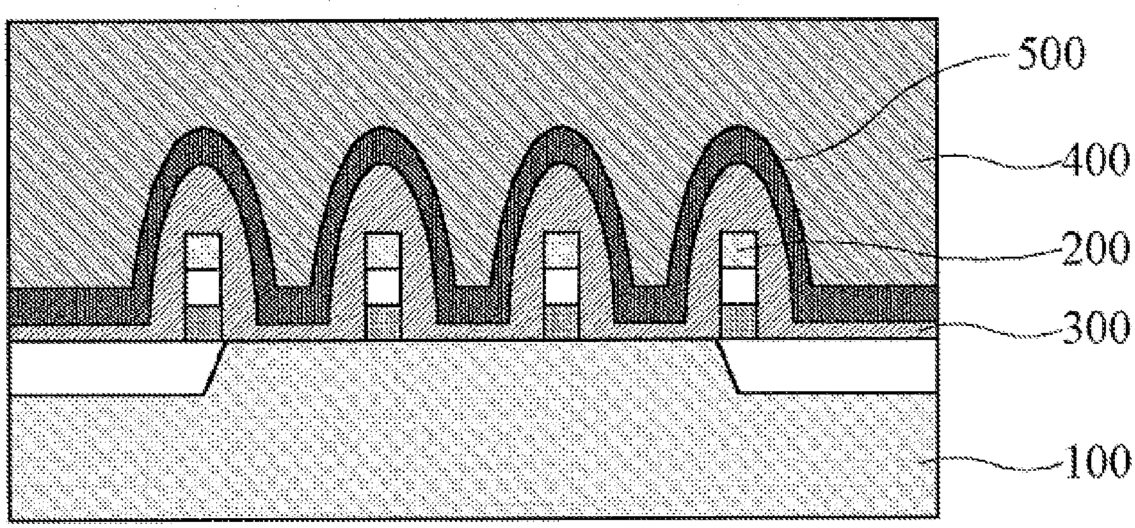

Figure 1

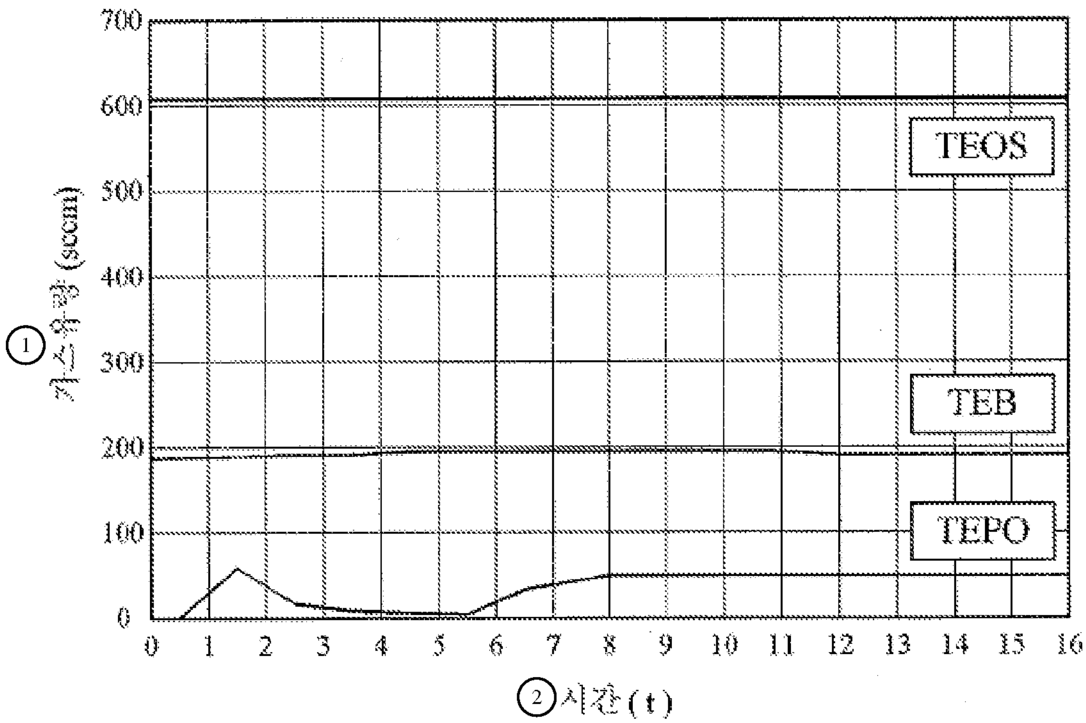

Figure 2

Key: 1 Amount of gas flow (sccm)

2 Time (t)

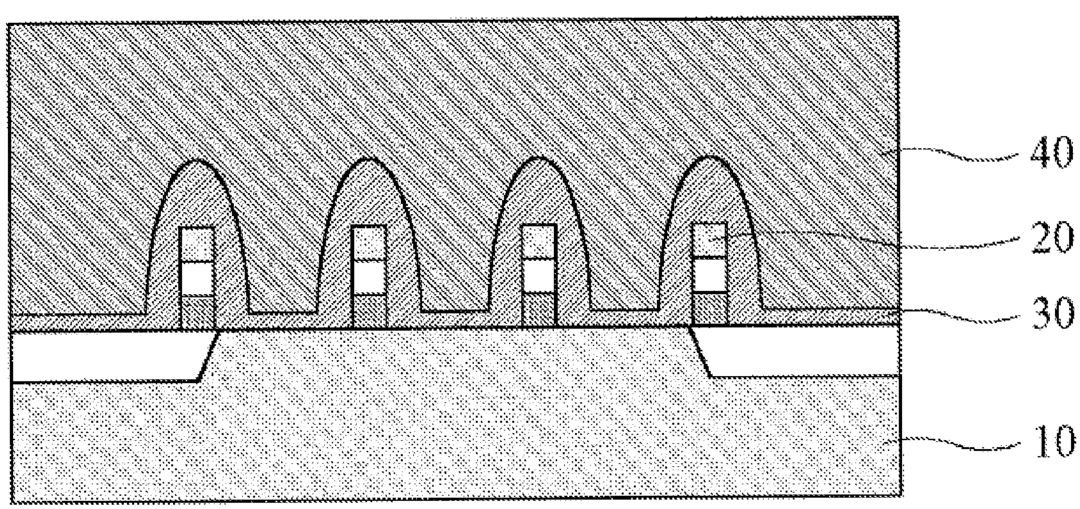

Figure 3

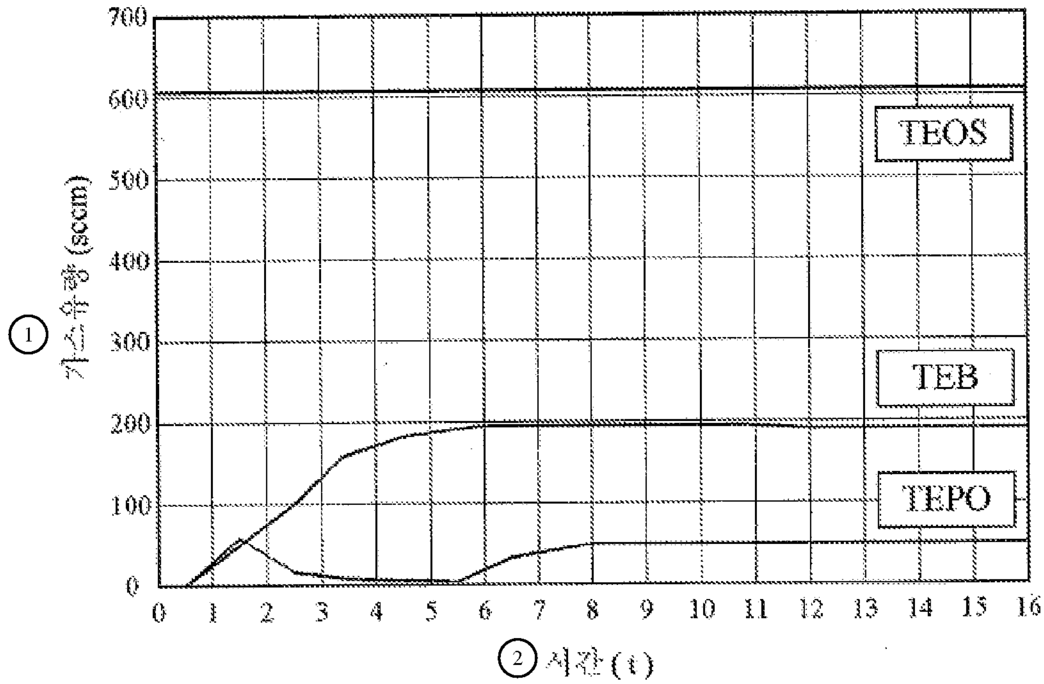

Figure 4

Key: 1 Amount of gas flow (sccm)

2 Time (t)